What is claimed is:

1. A clock generator generating a refresh clock signal used in a refresh execution of a semiconductor, comprising:

a first MOS transistor diode-connected for outputting a first bias voltage, a source of the first MOS transistor being connected to a supply voltage;

a second MOS transistor diode-connected for outputting a second bias voltage, a source of the second MOS transistor being connected to ground voltage;

a bias current control means having a predetermined number of serial-connected diodes for serving as a resistance in inverse proportion to a temperature, wherein the bias current control means is coupled between the first MOS transistor and the second MOS transistor to control the first and second bias voltages by using the resistance; and

a refresh clock generator generating the refresh clock signal having the frequency which is controlled or adjusted based on the first and second bias voltages.

2. The clock generator of claim 1, wherein the predetermined number is greater than value which divides the supply voltage by a threshold voltage of the diode.

3. The clock generator of claim 2, wherein the predetermined number is at least four.

4. The clock generator of claim 2, wherein each serial-connected diode is a diode-connected PMOS transistor.

5. The clock generator of claim 2, wherein each serial-connected diode is a diode-connected NMOS transistor.

6. The clock generator of claim 2, wherein the refresh clock generator is configured by using a ring oscillator having a number of inverters.

7. The clock generator of claim 6, wherein the inverter includes:

a third MOS transistor for building a current mirror with the first MOS transistor, source of the third MOS transistor is connected to the supply voltage and gate of the third MOS transistor is connected to gate of the first MOS transistor; and

a forth MOS transistor for building a current mirror with said the second MOS transistor, source of the forth MOS transistor is connected to the ground voltage and gate of the forth MOS transistor is connected to gate of the second MOS transistor.

8. The clock generator of claim 1, wherein an operating voltage of the serial-connected diodes included in the bias current control means is varied between a threshold voltage and a ZTC point.

9. A semiconductor device having a refresh operation unit for performing a refresh operation in response to a refresh clock, comprising:

a first MOS transistor diode-connected for outputting a first bias voltage, a source of the first MOS transistor being connected to a supply voltage;

a second MOS transistor diode-connected for outputting a second bias voltage, a source of the second MOS transistor being connected to ground voltage;

a bias current control means having a predetermined number of serial-connected diodes for serving as a resistance in inverse proportion to a temperature, wherein the bias current control means is coupled between the first MOS transistor and the second MOS transistor to control the first and second bias voltages by using the resistance; and

a refresh clock generator generating the refresh clock signal having the frequency which is controlled or adjusted based on the first and second bias voltages.

10. The semiconductor device of claim 9, wherein the predetermined number is greater than value which divides the supply voltage by a threshold voltage of the diode.

11. The semiconductor device of claim 10, wherein the predetermined number is at least four.

12. The semiconductor device of claim 10, wherein each serial-connected diode is a diode-connected PMOS transistor.

13. The semiconductor device of claim 10, wherein each serial-connected diode is a diode-connected NMOS transistor.

14. The semiconductor device of claim 10, wherein the refresh clock generator is configured by using a ring oscillator having a number of inverters.

15. The semiconductor device of claim 14, wherein the inverter includes:

a third MOS transistor for building a current mirror with the first MOS transistor, source of the third MOS transistor is connected to the supply voltage and gate of the third MOS transistor is connected to gate of the first MOS transistor; and

a forth MOS transistor for building a current mirror with said the second MOS transistor, source of the forth MOS transistor is connected to the ground voltage and gate of the forth MOS transistor is connected to gate of the second MOS transistor.

16. The semiconductor device of claim 9, wherein an operating voltage of the serial-connected diodes included in the bias current control means is varied between a threshold voltage and a ZTC point.